AMENDMENTS TO THE SPECIFICATION

Please change the paragraph [0012] on page 3 as follows:

[0001] According to the present invention a method and a system is provided for efficiently coding test vectors for ICs in scan design and with build-in test hardware (BIT-HW), whereby the BIT-HW consists of a linear feedback shift register (LFSR) for pseudo-random pattern generation and means for pattern merging and distribution over scan chains. The method in particular includes the generation of an executable logic model representation of the physical BIT-HW, ~~her~~ here called BIT-Code.